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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,733	02/27/2004	John W. Curry	200314830-1	8425

22879 7590 07/31/2006

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EXAMINER	
MEHRMANESH, ELMIRA	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,733	CURRY, JOHN W.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Curry, for a "Detecting floating point hardware failures" filed February 27, 2004, has been examined.

Claims 1-27 are presented for examination.

Claims 1, 2, 5-7, 10-12, 23-27 are rejected under 35 USC § 102.

Claims 3, 4, 8, 9, 13-22 are rejected under 35 USC § 103.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5-7, 10-12, and 23-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Blomgren et al. (U.S. Patent No. 5,884,057).

As per claim 1, Blomgren discloses a method for testing floating point hardware in a processor while executing a computer program, comprising: executing a first set of code of said computer program without employing said floating point hardware, said first set of code having a first floating point instruction, thereby obtaining an emulated result (col. 6, lines 61-67 through col. 7, lines 1-10)

executing said first floating point instruction utilizing said floating point hardware, thereby obtaining a hardware-generated result (col. 5, lines 8-38 and col. 8, lines 29-46)

comparing said emulated result with said hardware-generated result (col. 7, lines 56-64).

As per claim 2, Blomgren discloses rendering said floating point hardware unavailable prior to said executing said first set of code of said computer program without employing said floating point hardware (col. 4, lines 24-43).

As per claim 5, Blomgren discloses rendering said floating point hardware unavailable includes writing a first predefined value into a register in said processor (col. 4, lines 44-48).

As per claim 6, Blomgren discloses rendering said floating point hardware available for executing instructions of said computer program prior to said executing said first floating point instruction utilizing said floating point hardware (col. 5, lines 8-38).

As per claim 7, Blomgren discloses rendering said hardware available includes writing a second predefined value into said register in said processor (col. 4, lines 44-48).

As per claim 10, Blomgren discloses obtaining said hardware-generated result includes obtaining a trap result after said first floating point instruction is executed

utilizing said floating point hardware (col. 7, lines 11-18).

As per claim 11, Blomgren discloses obtaining emulated result includes obtaining a hardware-generated trap result after said processor encounters said first floating point instruction while said floating point hardware is unavailable (col. 7, lines 11-18).

As per claim 12, Blomgren discloses computer program represents a field application program (col. 6, lines 37-44).

As per claim 23, Blomgren discloses an article of manufacture comprising a program storage medium having computer readable code embodied therein, said computer readable code being configured to test floating point hardware in a processor while executing a computer program, comprising: computer readable code for executing a first set of code of said computer program without employing said floating point hardware, said first set of code having a first floating point instruction, thereby obtaining an emulated result (col. 6, lines 61-67 through col. 7, lines 1-10)

computer readable code for executing said first floating point instruction utilizing said floating point hardware, thereby obtaining a hardware-generated result (col. 5, lines 8-38)

computer readable code for comparing said emulated result with said hardware-generated result (col. 7, lines 56-64).

As per claim 24, Blomgren discloses computer readable code for rendering said floating point hardware unavailable prior to said executing said first set of code of said computer program without employing said floating point hardware (col. 4, lines 24-43).

As per claim 25, Blomgren discloses computer readable code for rendering said floating point hardware unavailable includes computer readable code for writing a first predefined value into a register in said processor (col. 4, lines 44-48).

As per claim 26, Blomgren discloses computer readable code for rendering said floating point hardware available for executing instructions of said computer program prior to said executing said first floating point instruction utilizing said floating point hardware (col. 5, lines 8-38).

As per claim 27, Blomgren discloses computer readable code for rendering said hardware available includes computer readable code for writing a second predefined value into said register in said processor (col. 4, lines 44-48).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3, 4, 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al. (U.S. Patent No. 5,884,057) in view of Markstein et al. (U.S. PGPUB 20040158600).

As per claim 3, Blomgren fails to explicitly disclose an Itanium.TM. processor.

Markstein teaches:

processor represents an Itanium.TM. processor, said rendering said floating point hardware unavailable including setting at least one of a DFH and a DFL bit in a processor status register of said processor (page 3, paragraph [0035] and [0036]).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method of emulation of floating point operations of Blomgren et al.'s in combination with the floating point computation method of Markstein et al.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Blomgren discloses a Dual-Instruction-Set Processor for RISC and CISC that can process integer and floating point instructions

from a first instruction set and from a second instruction set (Fig. 2 and Fig. 3). He also discloses of many modifications and variations to his invention (col. 10, lines 49-56). Markstein et al. discloses an Itanium.TM. processor for floating point operations (page 3, paragraph [0035] and [0036]).

As per claim 4, Blomgren fails to explicitly disclose a PA-RISC.TM. processor.

Markstein teaches:

processor represents a PA-RISC.TM. processor, said rendering said floating point hardware unavailable including clearing a CR10 co-processor control register of said processor (page 3, paragraph [0035] and [0036]).

As per claim 8, Blomgren fails to explicitly disclose an Itanium.TM. processor.

Markstein teaches:

processor represents an Itanium.TM.0 processor, said rendering said floating point hardware available including clearing at least one of a DFH and a DFL bit in a processor status register of said processor (page 3, paragraph [0035] and [0036]).

As per claim 9, Blomgren fails to explicitly disclose a PA-RISC.TM. processor.

Markstein teaches:

processor represents a PA-RISC.TM. processor, said rendering said floating point hardware available including setting a CR10 co-processor control register of said processor (page 3, paragraph [0035] and [0036]).

Claims 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al. (U.S. Patent No. 5,884,057) in view of Van Dyke et al. (U.S. Patent No. 7,047,394) and further view of Markstein et al. (U.S. PGPUB 20040158600).

As per claim 13, Blomgren discloses a method for detecting failure in floating point hardware of a processor while executing a computer program, comprising:, including executing a first floating point operation of said computer program by emulating said floating point operation with a set of non-floating point operations, thereby obtaining an emulated result (col. 6, lines 61-67 through col. 7, lines 1-10)

executing said first floating point operation utilizing said floating point hardware, thereby obtaining a hardware-generated result (col. 5, lines 8-38)

and comparing said emulated result with said hardware-generated result to detect said failure to detect said failure (col. 8, lines 29-46)

Blomgren fails to explicitly disclose a diagnostic mode.

Van Dyke teaches:

entering a diagnostic mode (col. 52, lines 29-44)

determining whether diagnostic mode is to be continued; and resuming execution of said computer program in a non-diagnostic mode if said diagnostic mode is to be discontinued, said non-diagnostic mode involving performing floating point operations of said computer program without emulating with non-floating point operations (col. 140, lines 44-64).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the method emulation of floating point operations of Blomgren et al.'s in combination with the floating point computation processor of Van Dyke et al.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Blomgren discloses a Dual-Instruction-Set Processor for RISC and CISC that can process integer and floating point instructions from a first instruction set and from a second instruction set (Fig. 2 and Fig. 3). He also discloses of many modifications and variations to his invention (col. 10, lines 49-56). Van Dyke et al. discloses a first operating system coded in a RISC instruction set and a second operating system coded in a CISC instruction set (col. 22, lines 51-59).

As per claim 14, Blomgren discloses rendering said floating point hardware unavailable prior to said executing said first floating point operation by said emulating (col. 4, lines 24-43).

As per claim 15, Blomgren in view of Van Dyke fails to explicitly disclose an Itanium.TM. processor.

Markstein teaches:

processor represents an Itanium.TM. processor, said rendering said floating point hardware unavailable including setting at least one of a DFH and a DFL bit in a

processor status register of said processor (page 3, paragraph [0035] and [0036]).

As per claim 16, Blomgren in view of Van Dyke fails to explicitly disclose a PA-RISC.TM. processor.

Markstein teaches:

processor represents a PA-RISC.TM. processor, said rendering said floating point hardware unavailable including clearing a CR10 co-processor control register of said processor (page 3, paragraph [0035] and [0036]).

As per claim 17, Blomgren discloses rendering said floating point hardware unavailable includes writing a first predefined value into a register in said processor (col. 4, lines 44-48).

As per claim 18, Blomgren discloses rendering said floating point hardware available for executing instructions of said computer program prior to said executing said first floating point operation utilizing said floating point hardware (col. 5, lines 8-38).

As per claim 19, Blomgren discloses hardware available includes writing a second predefined value into said register in said processor (col. 4, lines 44-48).

As per claim 20, Blomgren in view of Van Dyke fails to explicitly disclose an Itanium.TM. processor.

Markstein teaches:

processor represents an Itanium.TM. processor, said rendering said floating point hardware available including clearing at least one of a DFH and a DFL bit in a processor status register of said processor (page 3, paragraph [0035] and [0036]).

As per claim 21, Blomgren in view of Van Dyke fails to explicitly disclose a PA-RISC.TM. processor.

Markstein teaches:

processor represents a PA-RISC.TM. processor, said rendering said floating point hardware available including setting a CR10 co-processor control register of said processor (page 3, paragraph [0035] and [0036]).

As per claim 22, Blomgren discloses hardware-generated result includes obtaining a trap after said first floating point operation is executed utilizing said floating point hardware (col. 7, lines 11-18).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Ackerman et al. (U.S. Patent No. 5,606,696), "Exception handling method and apparatus for a microkernel data processing system".

Garg et al. (U.S. Patent No. 5,560,035), "RISC microprocessor architecture implementing multiple typed register sets".

Mirani et al. (U.S. Patent No. 6,434,741), "Method and apparatus for debugging of optimized code using emulation".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).